PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL9100

VIDEOTEXT DATA SLICER AND CLOCK REGENERATOR

The SL9100 has been designed to recover data from composite video type signals, e.g. Teletext broadcasts. As well as retrieving data, the SL9100 will resynchronise a Clock output to the Data stream and also provide a composite sync output.

FEATURES

- Slicing Of Data Adapts To Both The Black And White Video Levels
- Pre-Adaption Of The White Level Occurs At The Beginning Of Each Video Line
- Pre-Adaption Avoids Slicing Of The Colour Burst Signal
- TTL Compatible Data Output
- TTL Compatible Resynchronised Clock Output
- TTL Compatible Composite Sync Output
- Interfaces Directly To The Plessey Teleview System, Specifically The MR9710 And MR9735

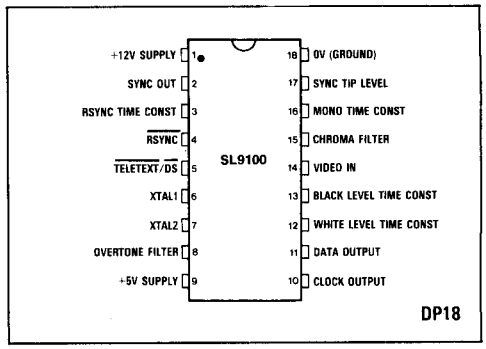

Fig.1 Pin connection - top view

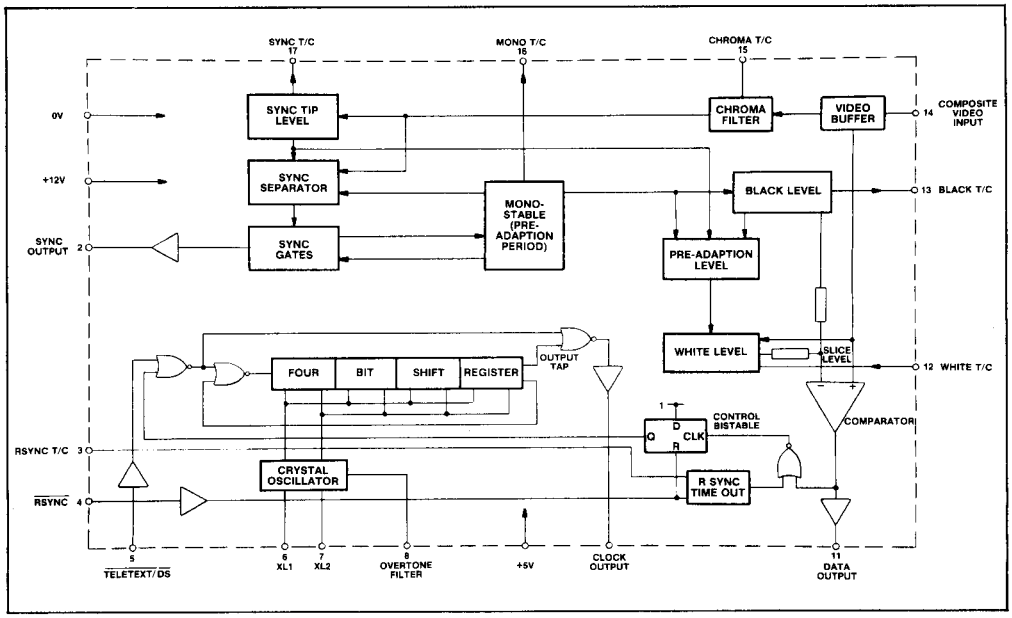

Fig.2 SL9100 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} = 25° C

Characteristic	Pin No. (Symbol)	Value			Unit	Conditions
		Min.	Typ.	Max.		
5V supply voltage	9	4.2		5.8	V	
5V supply current	9		40	45	mA	5V rail = 5V
12V supply voltage	1	10.8		13.2	V	
12V supply current	1		11	15	mA	12V rail = 12V
Video input (p-p)	14	1.5		4.5	V	AC coupled, positive video
Input impedance	14		10		kΩ	
Signal/noise ratio	14	20			dB	W.R.T. data height, during data line, with band limited white noise
Co-channel interference	14		130		mV(pk)	26.042kHz sine wave added to video
Co-channel interference	14		130		mV(pk)	52.083kHz sine wave added to video
$\overline{\text{RSYNC}}$ input pull-up	4	3.0			kΩ	Internal to +5V
$\overline{\text{RSYNC}}$ input low level	4			0.5	V	0.5mA max. source
$\overline{\text{RSYNC}}$ input high level	4	4.8			V	20μA max. source from pin
$\overline{\text{RSYNC}}$ input capacitance	4			5	pF	
$\overline{\text{Teletext/DS}}$ pull-up	5		10		kΩ	Internal to +5V
$\overline{\text{Teletext/DS}}$ input low	5			0.5	V	500μA max. source
Sync output low level	2			0.4	V	
Sync output high level	2	3.5			V	
Data output low level	11			0.4	V	Sink 1.5mA min. } Drive
Data output high level	11	3.0			V	Source 1.5mA min. } 25pF max.
Clock output low level	10			0.4	V	Sink 1.5mA min. } Drive
Clock output high level	10	3.5			V	Source 1.5mA min. } 25pF max.
Black level source	13		25		μA	
White level sink	12		25		μA	
Mono source	16		50		μA	
Sync tip level source	17		20		μA	
Pre-adaption	12	60		100	%	Over video input range
Data slice level	(11)		50		%	Over video input range
Sink slice level	(14)		150		mV	Level above sync tips at pin 14
Crystal oscillator frequency (fx)	6/7		55.5		MHz	Components as in Fig.5
Clock output frequency	10	1.5	fx/8	7.5	MHz	Free running (no video input)
Data output frequency	11	1.5		7.5	MHz	
Regenerated clock phase	10	60		90	ns	Trailing edge lag w.r.t. data output trailing edge

CIRCUIT DESCRIPTION

Video Input (Pin 14) And Chroma Time Constant (Pin 15)

The incoming video is AC-coupled into an emitter follower, biased to 6.4V through 10kΩ. This provides 'buffered video' which is then fed to an external pad through 1kΩ, where an external capacitor (C8 = 1nF) acts as a single pole filter. This filter subdues the chrominance signal, providing 'filtered video', after correcting for the voltage drop in the 1kΩ resistor.

Sync Time Constant (Pin 17) And Sync Output (Pin 2)

'Filtered video' is fed into a conventional negative peak detector using a current source into an external capacitor (C10 = 22nF). The output of this is modified in two ways:

1. With no signal present, it is clamped typically 0.2V below the quiescent video level, ensuring no SYNC output or
2. With SYNC detected the output will represent a SYNC slice level typically 0.15V above the SYNC tips (positive video).

This provides slicing of 'filtered video' which produces positive SYNC's at ECL levels for internal use. This signal is then inverted in a TTL output buffer, producing negative going composite SYNC.

Monostable Time Constant (Pin 16)

This provides the 'pre-adaption period' which has the following functions:

1. To determine when pre-adaption takes place and
2. Clamp a capacitor to the black level for subsequent reference.

The monostable is triggered on the trailing SYNC edge with a typical period of 4μs. This is set by an external capacitor (C9 = 100pF) on pin 16.

The associated SYNC gates ensure that slicing of the colour burst, or other noise immediately following SYNC, does not give rise to a false SYNC pulse or pre-adpation period. Fig.3 shows the resultant action.

Black Level Time Constant (Pin 13) And Pre-Adaption Level

The black level circuit comprises two separate peak detectors. The first tracks negative excursions of DATA in the video signal, while the positive detector resets the black level during the pre-adaption period. The positive detector is normally gated out. The negative peak detector includes a current source which charges the external black level time constant capacitor (C6 = 2.2nF) on pin 13.

During the pre-adaption period, a fixed gain amplifier is enabled to produce a 'pre-adaption level'.

A voltage proportional to the SYNC height w.r.t. black level is added to the black level and fed to the white level circuitry (i.e. estimated data size).

White Level Time Constant (Pin 12) And Data Output (Pin 11)

The white level is determined by a positive peak detector which stores either the most positive data level, or estimated data level (pre-adaption). The white level time constant is determined by an external capacitor (C5 = 2.2nF, pin 12) which is drained by an internal current sink.

The mean value of both black and white levels is chosen to be the slice level at which DATA is recovered from the video signal. This mean level is normally set at 50% of the difference of black and white levels as indicated by the two resistors shown in Fig.2. The DATA, at ECL levels, is used for Clock regeneration and also feeds a TTL buffer for output at pin 11.

Crystal Oscillator (Pins 6 And 7) And Overtone Filter (Pin 8)

The crystal oscillator uses a third overtone crystal and a parallel tuned circuit (pin 8) to ensure oscillation at 55.5MHz. It provides two anti-phase clocks for driving an on-chip four-bit shift register.

Clock Output (Pin 10) And $\overline{\text{Teletext}}/\overline{\text{DS}}$ (Pin 5)

The crystal oscillator output is divided by eight by the 4-bit shift register to provide a 7MHz (typ.) clock from incoming data. The output of the control bistable provides synchronisation of the regenerated clock to the recovered data.

When the control bistable output and $\overline{\text{Teletext}}/\overline{\text{DS}}$ pin are both low, the shift register will fill with zeros. Note that DS is grounded for Teletext operation, and that an $\overline{\text{RSYNC}}$ pulse will reset the control bistable output to zero. The output of the first NOR gate associated with the register will hold the clock output to zero until a negative transition of Data clocks the control bistable. This NOR gate output will then go low, allowing the zeros in the register to be clocked out as ones, and also fed back to the input and re-loaded as ones. This provides resynchronisation, and the output tap on the shift register is such that the negative clock edge occurs during the middle of each Data bit to provide correct clock phase w.r.t. recovered data.

Note that if the $\overline{\text{Teletext}}/\overline{\text{DS}}$ pin is held high, the clock output is a free-running division of the 55.5MHz oscillator.

$\overline{\text{RSYNC}}$ Input (Pin 4) And RSYNC Time Constant (Pin 3)

Clock resynchronisation takes place at the start of each line. An $\overline{\text{RSYNC}}$ pulse will occur at the beginning of each possible Teletext line. If data is present, the clock is re-started, checked for frequency by the Teleview system and a second $\overline{\text{RSYNC}}$ pulse occurs to provide final resynchronisation (see Timing Diagram, Fig.4). If, on a possible Teletext line, no data is present then the $\overline{\text{RSYNC}}$ time-out circuit provides re-start of the clock before the end of the line (typically 20μs after the last $\overline{\text{RSYNC}}$ pulse). This uses an external capacitor (C1 = 1nF) on pin 3, pulled up through a 20kΩ resistor, which is discharged by each $\overline{\text{RSYNC}}$ pulse.

APPLICATION NOTES

Black And White Time Constants

The black and white time constants are set by the external capacitors, C6 and C5 respectively, and the internal source and sink currents of 25μA, on pins 13 and 12. The values of C6 and C5 can be calculated once the rate at which the levels must change, in order to accommodate signal level fluctuations, has been pre-determined.

For the white level, an additional restriction must be taken into account in order to avoid false data to be sliced. This level must not fall to that of the black level, within a line period, or it will be similar to the quiescent black level, and hence the data slice level also. In order to be safe, this means that the value of C5 should not be less than 2.2nF.

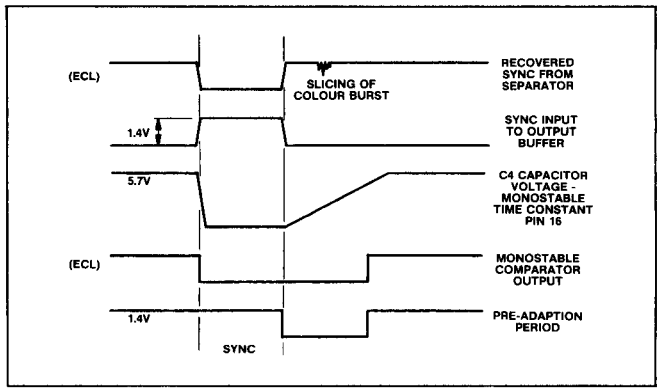

Fig.3 SYNC and monostable timing

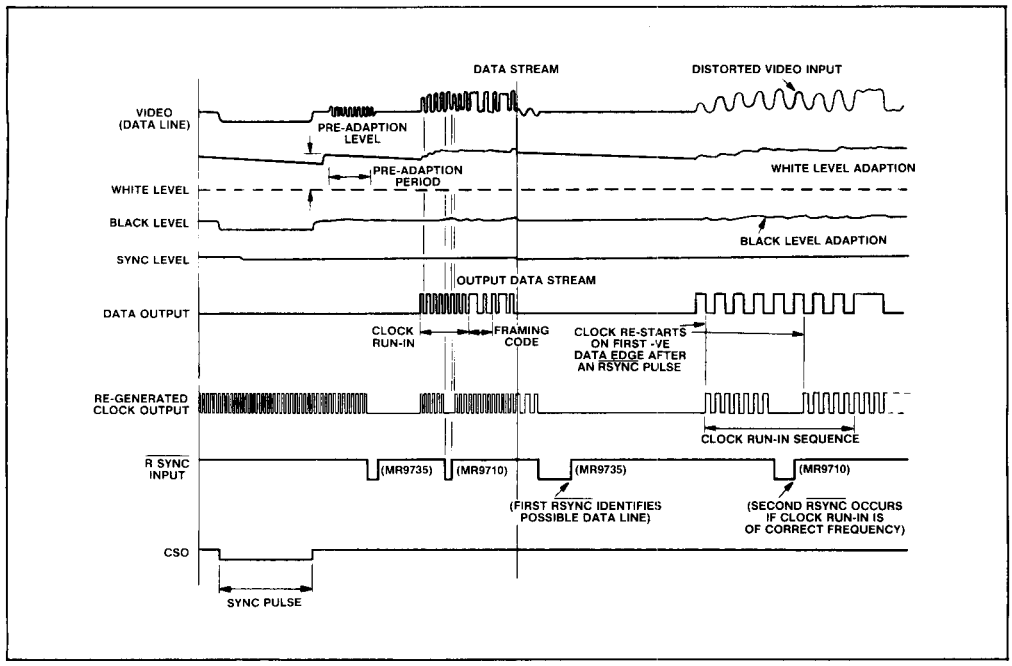

Fig.4 SL9100 timing diagram showing RSYNC input timing and clock re-synchronisation (for Teleview system)

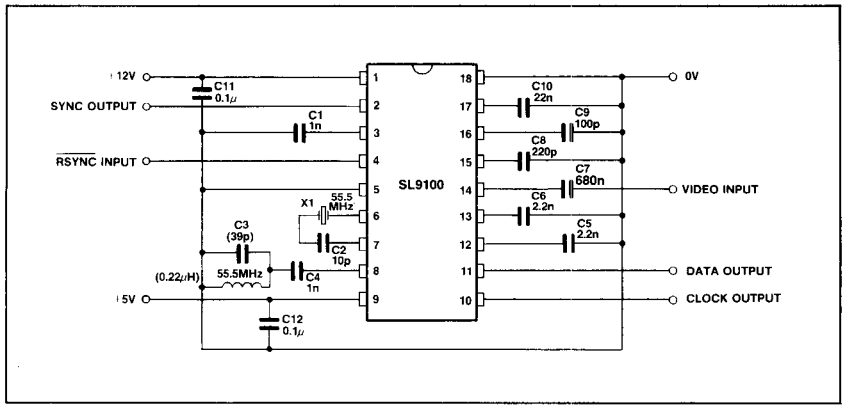

Fig.5 Application circuit showing external components